WHAT IS CLAIMED IS:

1. An integrated circuit that implements a (2,k)-regular low-density parity check code decoder with the functionality of 2Lk check node functions and $Lk^2$ variable node functions, comprising:

   (a) $k^2$ random access memories (RAMs),

   (b) $k^2$ variable node units, wherein one variable node unit is coupled to one RAM,

   (c) a bidirectional shuffle network connected to the said $k^2$ RAMs,

   (d) k check node units connected to the said shuffle network, and

   (e) $k^2$ modulo-L counters, wherein each modulo-L counter is an address generator for one RAM.

2. An integrated circuit that implements a (3,k)-regular low-density parity check code decoder with the functionality of 3Lk check node functions and $Lk^2$ variable node functions, comprising:

   (a) $k^2$ random access memories (RAMs),

   (b) $k^2$ variable node units, wherein one variable node unit is coupled to one RAM,

   (c) a first bidirectional shuffle network that is connected to the said RAMs,

   (d) a second bidirectional shuffle network coupled to the first bidirectional shuffle network, wherein the permutations performed by the second shuffle network are controlled by a g-bit word,

   (e) a random pattern generator which is coupled to the said second shuffle network wherein the random pattern generator generates the g-bit word to control the permutations in the second shuffle network,

   (f) k check node units connected to the said second shuffle network, and

(g) $k^2$ modulo-L counters, wherein each modulo-L counter is an address generator for one RAM.

3. An integrated circuit that implements a (3,k)-regular low-density parity check code decoder with the functionality of 3Lk check node functions and $Lk^2$ variable node functions, comprising:

(a) $k^2$ random access memories (RAMs),

(b) $k^2$ variable node units, wherein one variable node unit is coupled to one RAM,

(c) a first bidirectional shuffle network that is connected to the said RAMs, wherein the permutations performed by the shuffle network are regular and fixed,

(d) a second bidirectional shuffle network that is connected to the said RAMs, wherein the permutations performed by the said shuffle network are regular and fixed,

(e) a third bidirectional shuffle network that is connected to the said RAMs, wherein the permutations performed by the said shuffle network are random-like and configurable,

(f) k check node units connected to the first shuffle network,

(g) k check node units connected to the second shuffle network,

(h) k check node units connected to the third shuffle network,

(i) $k^2$ modulo-L counters, wherein each modulo-L counter is an address generator for one RAM.

4. The integrated circuit of claim 1, wherein the variable node unit retrieves a channel message and 2 check-to-variable messages from the RAM to which it is coupled, and computes 2 variable-to-check messages, and stores the said messages in the RAMs, in every clock cycle.

5. The integrated circuit of claim 1, wherein k check node units retrieve $k^2$ variable-to-check messages from the RAMs after shuffling, compute $k^2$ check-to-variable messages,

and store them back in the RAMs after unshuffling.

6. The integrated circuit of claim 1, wherein the shuffle network performs permutations in first L cycles, and performs no permutations in next L cycles.

7. The integrated circuit of claim 2, wherein the variable node unit retrieves a channel message and 2 check-to-variable messages from the RAM to which it is coupled, and computes 2 variable-to-check messages, and stores the said messages in the RAMs.

8. The integrated circuit of claim 1, wherein k check node units retrieve $k^2$ variable-to-check messages from the RAMs after shuffling, compute $k^2$ check-to-variable messages, and store them back in the RAMs after unshuffling.

9. The integrated circuit of claim 2, wherein the first shuffle network performs permutations in the first L clock cycles and performs no permutations in second and third L clock cycles.

10. The integrated circuit of claim 2, wherein the second shuffle network performs no permutations in first and second L clock cycles, and performs permutations in 3rd L clock cycles.

11. The integrated circuit of claim 2, wherein the random pattern generator performs a hash function.

12. The integrated circuit of claim 2 as part of a wireless transceiver.

13. The integrated circuit of claim 2 as part of a storage system.

14. The integrated circuit of claim 2 as part of a communications receiver.

15. The integrated circuit of claim 3, wherein the check node units compute check-to-variable messages in the first L cycles.

16. The integrated circuit of claim 3, wherein the variable node units compute variable-to-check messages in second L cycles.

17. The integrated circuit of claim 3 as part of a wireless system.

18. The integrated circuit of claim 3 as part of a storage system.

19. The integrated circuit of claim 3 as part of a communications receiver.